IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331, Volume 11, Issue 6 Ver. I (Nov. – Dec. 2016), PP 64-69
www.iosrjournals.org

Design Analysis and Simulation of UPQC-I to Mitigate Power Quality Problems

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Abstract: *The unified power-quality conditioner (UPQC) is used to mitigate the current and voltage-related power-quality (PQ) problems simultaneously in power distribution systems. This paper proposes a new connection of UPQC between two parallel feeders called UPQC-I (Interline Unified power quality conditioner) to mitigate the power quality problems on two parallel feeders. In this analysis, one of the feeder supplies power to the non-linear load (L1) and another line supplies power to the sensitive load that requires uninterrupted and regulated voltage. A detailed mathematical analysis, to develop UPQC-I, is presented in this paper. MATLAB/SIMULINK-based simulation results are discussed to support the developed configuration.*

Keywords: *power quality, reactive power compensation, unified power quality conditioner (UPQC), Interline Unified power quality conditioner (UPQC-I), Shunt converter and series converter voltage sag and swell compensation, Active power filters (APF),controller*

I. Introduction

The different power quality problems arise in present modern power system. The main reasons for power quality problems are due to the extensive use of nonlinear loads, the penetration level of small/large-scale renewable energy systems based on wind energy, solar energy, fuel cell, etc., installed at distribution as well as transmission systems, faults like open circuits and short circuits, capacitance switching, lightning effects, loading effects etc…[1], [2]. To maintain the controlled power quality regulations some kind of compensation at all the power levels is becoming a common practice [5]–[9]. At the distribution level, UPQC is a most attractive solution to compensate several major power quality problems [7]–[9], [14]–[28]. The UPQC is composed with two active filters i,e.. Two 3-leg voltage source inverters (VSI) connected back to back with dc link capacitor. Functionally, the series filter is used to compensate for the voltage distortions like voltage sag, voltage swell, under voltages, over voltages etc.. While the shunt filter is needed to provide the reactive power and counteract the harmonic current injected by the load. Also the voltage of the dc link capacitor is controlled to a desired value by the shunt active filter. The general block diagram representation of a UPQC-based system is shown in Fig. 1. The voltage sag/swell on the system is one of the most important power quality problems [1], [2]. The voltage sag/swell can be effectively compensated using a dynamic voltage restorer, series active filter, UPQC, etc. [7]–[28]. Among the available power quality enhancement devices, the UPQC has better sag/swell compensation capability. .

II. System Configuration Of Interline Unified Power Quality Conditioner (UPQC-I)

The voltage at PCC1 and PCC2 may be or may not be distorted depending on the other non-linear loads connected at PCC1 and PCC2. Also, these loads may impose the voltage Sag/Swell conditions during their switching ON and/or OFF operation. The UPQC-I is installed between two parallel feeders to protect a sensitive loads at load buses 1 and 2 from all disturbances. In this proposed scheme, the UPQC consists of two active filters connected back to back with dc coupling; one APF which is called series APF is connected in series with the feeder which supplies power to sensitive loads that requires Uninterrupted and regulated voltage. The other APF called shunt APF is connected in parallel with the non-linear load which is supplied by the second feeder. The general block diagram of a proposed Interline unified power quality conditioner (UPQC-I) is shown in figure 2.

III. Steady State Power Flow Analysis Of UPQC-I

The powers due to harmonics are negligible as compared to the power at fundamental component, therefore the harmonic power is neglected and the steady state operating analysis is done on the basis of fundamental frequency component only. The UPQC-I is controlled in such a way that the voltage at load bus 2 and 1 is always sinusoidal and at desired magnitude. Therefore the voltage injected by series APF must be equal to the difference between the supply voltage at feeder line 1 and the ideal load voltage. Thus the series APF act as controlled voltage source. The function of shunt APF is maintain the dc link voltage at constant level. In addition to this the shunt APF provides the VAR required by the load, such that the input power factor will be

input and only fundamental active power supplied by the source. The voltage injected by series APF can vary 0_o to 360^0. Depending on the voltage injected by series APF, there can be a phase angle difference between the load voltage and the source voltage. However, in changing phase angle of series APF, the amplitude of voltage injected increase, thus increasing the required KVA rating of series APF. In the following analysis the load voltage is assumed to be in phase with terminal voltage even during voltage sag and swell condition. This is done by injecting the series voltage in phase or out of phase with respective to the source voltage during voltage sag and swell condition respectively. This suggests the real power flow through the series APF. The voltage injected by series APF could be positive or negative, depending on the source voltage magnitude, absorbing or supplying the real power. In this particular condition, the series APF could not handle reactive power and the load reactive power at load bus 2 is supplied by shunt APF alone. The per phase equivalent circuit for a 3-phase UPQC-I is shown in figure 3. The source voltage at feeder line1, terminal voltage at PCC_1, load voltage at load bus L_1, source current at feeder line 1 and load current at load bus L_1 are denoted by v_{s1}, v_{t1}, v_{l1}, i_{s1} and i_{l1}. Similarly The source voltage at feeder line 2, terminal voltage at PCC_2, load voltage at load bus L_2, source current at feeder line 2 and load current at load bus L_2 are denoted by v_{s2}, v_{t2}, v_{l2}, i_{s2} and i_{l2}. The voltage injected by series APF is denoted by v_{sr}, whereas the current injected by shunt APF is denoted by i_{sh}. Taking the Load voltage v_{l1} as a reference phasor and suppose the lagging power factor of the load is $\cos\phi_1$, then we can write,

$v_{l2} = v_{l2} < 0^0$ (1)

$i_{l1} = i_{l1} < \phi_{l1}$ (2)

$v_{l2} = v_{l2}(1 + k) < 0^0$ (3)

Where factor k represents the fluctuation of source voltage defined as

$k = \frac{v_{t2} - v_{l2}}{v_{l2}}$ (4)

The series injected by series inverter must be equal to,

$v_{sr} = v_{t2} - v_{l2} = -kv_{l2} < 0^0$ (5)

The UPQC-I is assumed to be loss less and therefore, the active power demanded by the load l2 is equal to the active power input at PCC2. The UPQC-I provides nearly unity power factor source current, therefore, for load condition the input power at PCC2 can be expressed by the following equations

$p_{t2} = p_{l2}$ (6)

$v_{t2} i_{s2} = v_{l2} i_{l2} \cos \emptyset_{l2}$ (7)

$v_{l2}(1 + k) i_{s2} = v_{l2} i_{l2} \cos \emptyset_{l2}$ (8)

$i_{s2} = \frac{i_{l2}}{1+k} \cos \emptyset_{l2}$ (9)

The above equation suggests that the source current i_{s2} depends on the factor k, since ϕ_{l2} and i_{l2} are load l_2 characteristics and are constant for a particular type of load.

The complex power absorbed by the series inverter can be expressed as

$s_{sr} = v_{sr} i_{s2}$ (10)

$P_{sr} = v_{sr} i_{s2} \cos \emptyset_{s2} = -kv_{l2} i_{s2} \cos \emptyset_{s2}$ (11)

$Q_{sr} = v_{sr} i_{s2} \cos \emptyset_{s2}$ (12)

ϕ_{s2}=0, since UPQC-I is maintaining unity power factor

$P_{sr} = v_{sr} i_{s2} = -kv_{l2} i_{s2}$ (13)

$Q_{sr} = 0$ (14)

The complex power absorbed by the shunt inverter can be expressed as

$s_{sh} = v_{l1} i_{sh}$ (15)

The current provided by the shunt inverter, is the difference between the input source current at feeder line1 and load current at load bus, which includes the load harmonics current and the reactive current. Therefore, we can write,

$i_{sh} = i_{s1} - i_{l1}$ (16)

$i_{sh} = i_{s1} < 0^0 - i_{l1}\phi_{l1}$ (17)

$i_{sh} = i_{s1} - (i_{l1} \cos \phi_{l1} - j i_{l1} \sin \phi_{l1})$ (18)

$i_{sh} = (\left(\left(i_{s1} - (i_{l1} \cos \phi_{l1}\right)\right) + j i_{l1} \sin \phi_{l1})$ (19)

$p_{sh} = v_{l2} i_{sh} \cos \emptyset_{sh} = v_{l1}\left(i_{s1} - (i_{l1} \cos \phi_{l1}\right)$ (20)

$Q_{sh} = v_{l1} i_{sh} \sin \emptyset_{sh} = v_{l1} i_{l1} \sin \emptyset_{l2}$ (21)

IV. UPQC-I Controller

In this paper, the generation of reference signals for series inverter and shunt inverter are discussed. Note that, as the series inverter maintains the load voltage of feeder line 1 and feeder line 2 at desired level, the reactive power demanded by the load at feeder line 2 remains unchanged (assuming load on the system is constant) irrespective of changes in the source voltage magnitude, but the reactive power demand by the load at

feeder line 1 is changes. The control block diagram for series inverter operation of UPQC-I is shown in figure below 8. The control block diagram for Shunt inverter operation of UPQC-I is shown in figure below 9

V. Figures And Tables

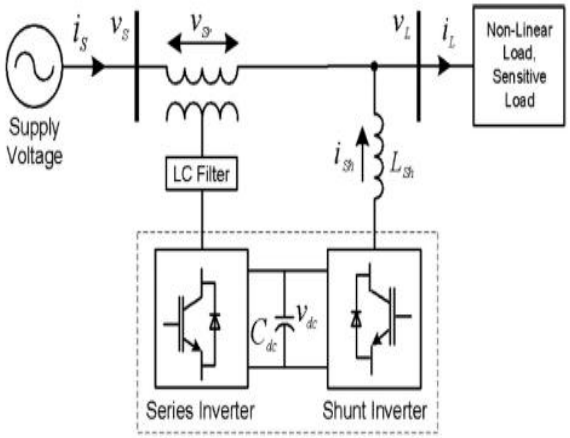

Fig.1: General Block diagram of Unified power quality conditioner (UPQC) system configuration

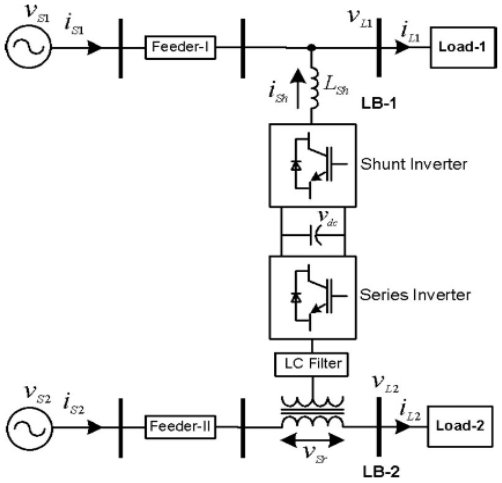

Fig.2: General block diagram of Interline unified power quality conditioner (UPQC-I).

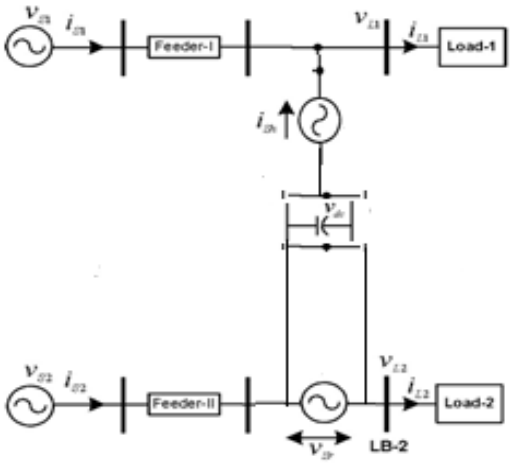

Fig.3: Equivalent circuit of an UPQC-I

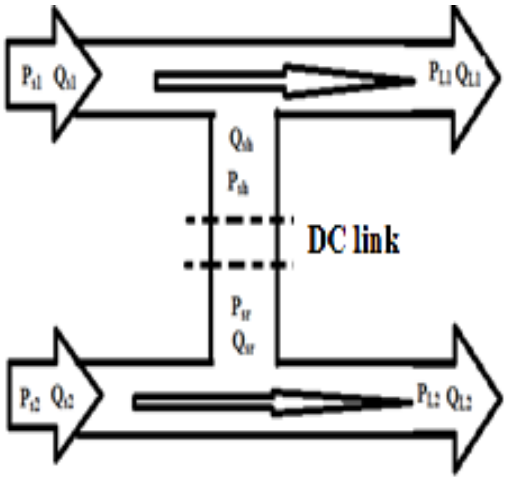

Fig.4: Active and Reactive power flow during normal working condition.

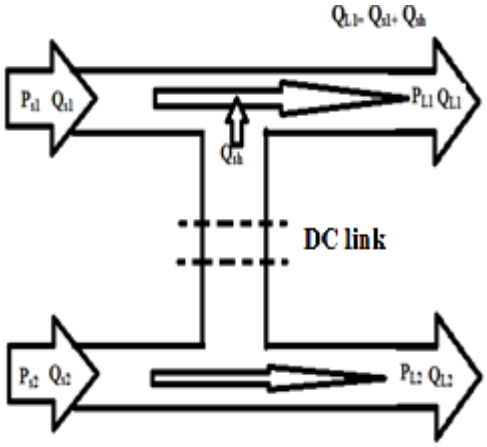

Fig.5: Reactive power flow when reactive power demand increases at Load bus 1

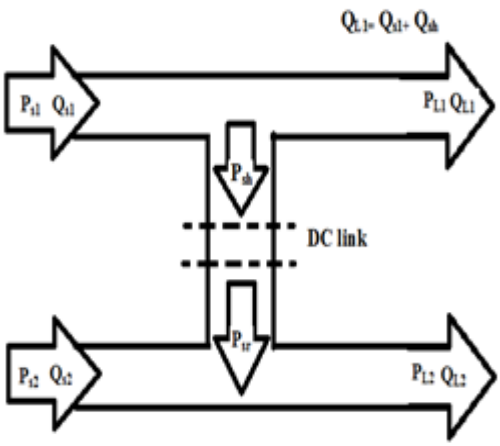

Fig.6: Active power flow during voltage sag condition

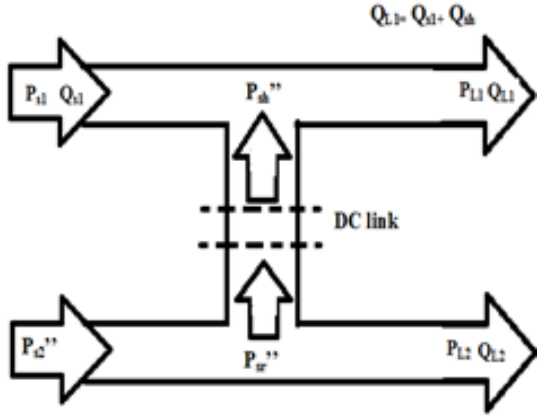

Fig.7: Active power flow during voltage swells condition

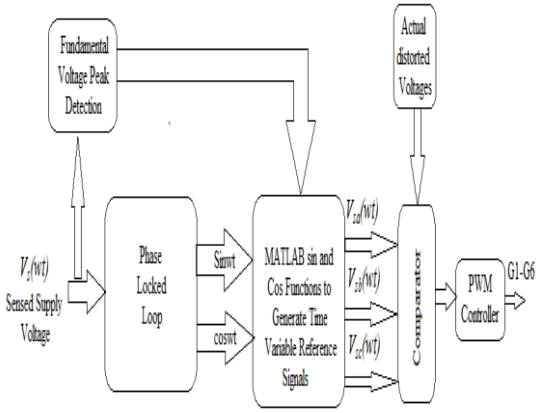

Fig.8: Reference voltage signal generation for the series inverter of the proposed UPQC-I

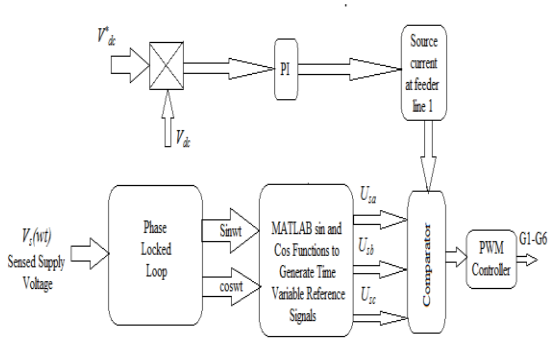

Fig.9: Reference voltage signal generation for the shunt inverter of the proposed UPQC-I

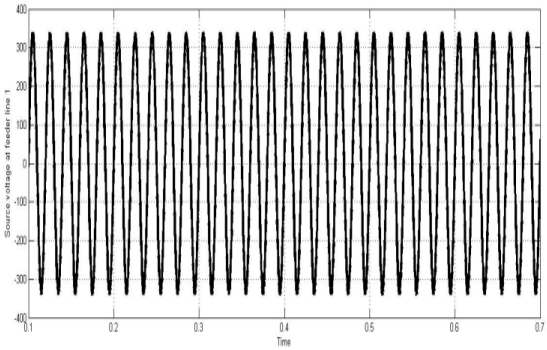

Fig.10a: Source voltage at feeder line1

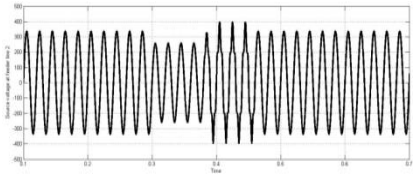

Fig.10b: Source voltage at feeder line2

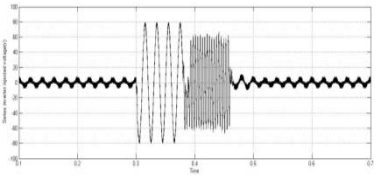

Fig.10c: Voltage injection by series inverter

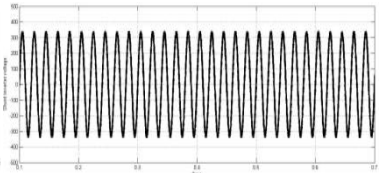

Fig.10d: Shunt inverter voltage

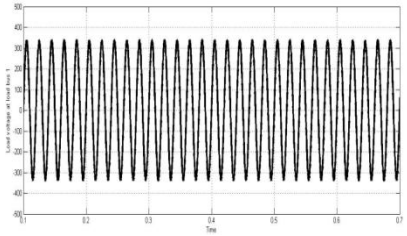

Fig.10e: Load voltage at Load bus 1

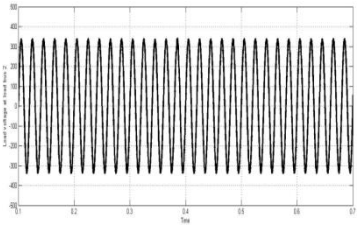

Fig.10f: Load voltage at Load bus 2

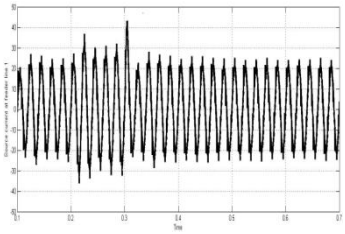

Fig.1g: Source current at feeder line1

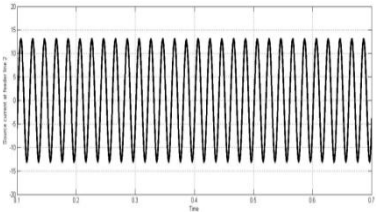

Fig.10h: Source current at feeder line2

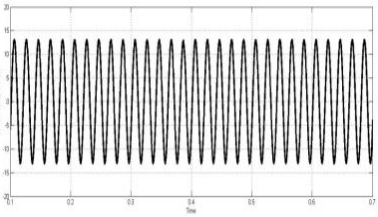

Fig.10i: Series inverter current

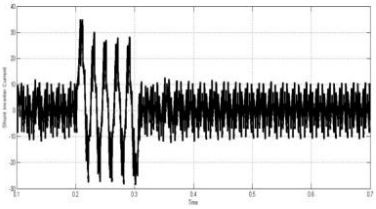

Fig.10j: Shunt inverter current

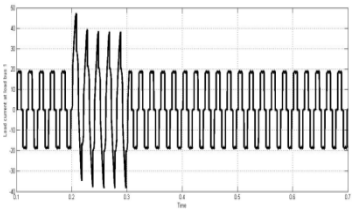

Fig.10k: Load current at Load bus 1

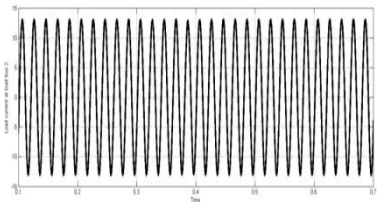

Fig.10l: Load current at Load bus 2

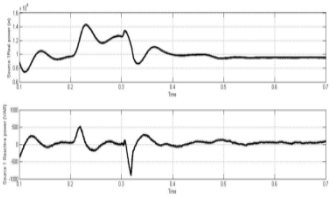

Fig.11a: Active and Reactive power at source

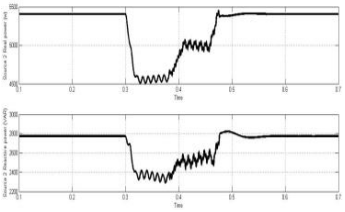

Fig.11b: Active and Reactive power at source2

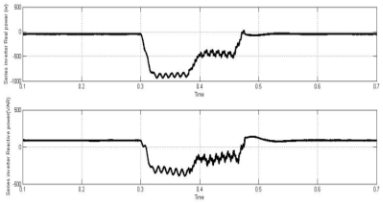

Fig.11c: Series inverter Active and Reactive power

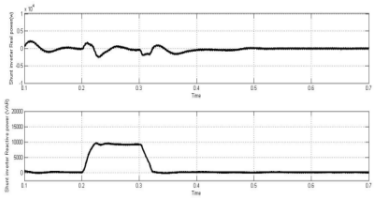

Fig.11d: Shunt inverter Active and Reactive power

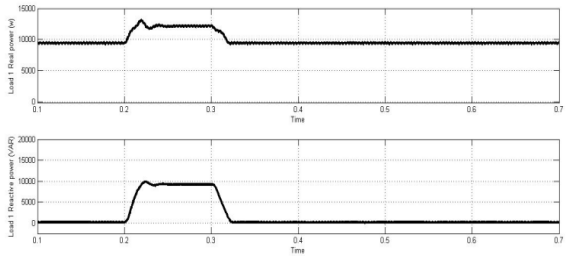

Fig.11e: Active and Reactive power at Load bus 1

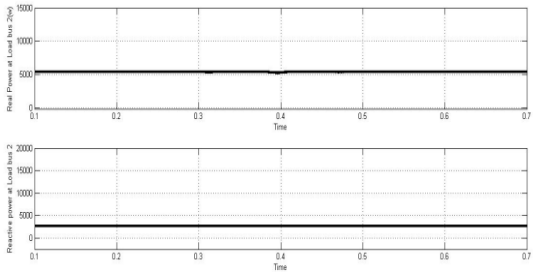

Fig.11f: Active and Reactive power at Load bus 2

VI. Simulation Results

The performance of the proposed UPQC-I for compensation of load reactive power at load bus 1 which is supplied by the feeder line 1 and voltage sag/swell at load bus 2 which is supplied by the feeder line 2 in the power system has been evaluated by simulation. To analyze the performance of proposed configuration of UPQC-I, the source at feeder line 1 and feeder line 2 is assumed to be pure sinusoidal. The simulation results of voltages and currents for the proposed configuration of UPQC-I are given in figure below 10. Source voltage at feeder line 2 have sag from time period t=0.3sec to t=0.38sec and swell from time period time period t=0.4sec to t=0.46sec is shown in figure below 10b.Source voltage at feeder line 1 is shown in figure 10a.The load at load bus 2 is R-L load (6000w, 3000VAR) and the load at load bus 2 is non-linear, sensitive load and R-L load. The real power and reactive power demand by load at load bus 2 is 9000w, 0VAR for time period of 0.1 sec to 0.2 sec, 12000w, 9000VAR for time period of 0.2sec to 0.3 sec and 9000w, 0VAR for time period of 0.3 sec to 0.7 sec. The current drawn by the load at load bus 1 is 20A peak from 0.1sec to 0.2 sec and 0.3sec to 0.7 sec, 38A peak from 0.2 sec to 0.3 sec is shown if figure 10k. The current drawn by the load L2 at load bus 2 is 12.5A peak is shown in figure 10i.The UPQC-I compensate the voltage sag/swell and reactive power demand by maintaining voltages at load bus 1 and load bus 2 are constant shown in figure 10e and 10f. The series inverter injects the voltage 80v peak for time period 0.3sec to 0.38 sec during voltage sag condition in phase and it injects a voltage 60v peak from time period of 0.4sec to 0.46sec during voltage swell conditions to maintain load voltage at load bus 2 constant is shown in figure 10c.The simulation results of real and reactive power flows between two parallel feeders when proposed configuration of UPQC-I is put into action to mitigate power quality problems are shown in figure below 11. The reactive power demand by the load at load bus 2 from 0.2sec to 0.3 sec is supplied by the shunt inverter by reducing the reactive power demand on the source 2 is shown in figure 11d.

VII. Conclusion

The steady state power flow analysis of UPQC-I is presented in this paper. The MATLAB/Simulink based simulations is done in order to verify the analysis proposed. The series APF injects in phase voltage

during voltage sag condition and out of phase during voltage swell condition at load bus 2 to maintains constant voltage. The shunt APF compensate reactive power demand by the load at load bus 1 and also it maintain dc link voltage constant level such that the series APF could effectively absorbs and delivers real power to mitigate power quality problems

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Examples follow:

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